



H3842S

HIGH PERFORMANCE CURRENT MODE CONTROLERS

Description

The H3842S is high performance fixed frequency current mode controllers. That is specifically designed for Off-Line and DC To DC converter applications offering the designer a costeffective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control. A temperature compensated reference, high gain error amplifier, current sensing compar-a-tor, and a high current totem pole output ideally suited for driving a power MOSFET. Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

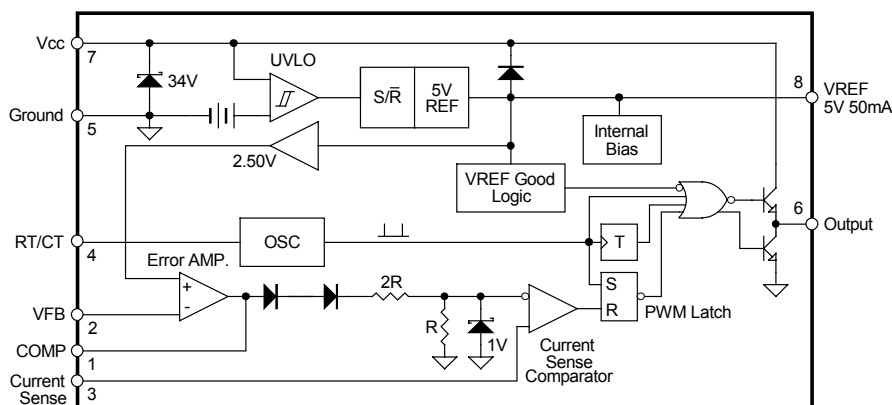
Features

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage ($I_i < 30\text{mA}$)	Self Limiting	
I_o	Output Current	± 1	A
E_o	Output Energy (capacitive load)	5	μJ
	Analog Inputs (pin 2, 3)	-0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{amb} \leq 25^\circ\text{C}$	800	mW
T_{stg}	Storage Temperature Range	-65 to 150	$^\circ\text{C}$
T_J	Junction Operating Temperature	-40 to 150	$^\circ\text{C}$
TL	Lead Temperature (soldering 10s)	300	$^\circ\text{C}$

Block Diagram





Pin Connection (Top View)

SOP-8P	Function	Description
	Pin1: Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
	Pin2: Voltage Feedback	This is the inverting input of the Error Amplifier. It's normally connected to the switching power supply output through a resistor divider.
	Pin3: Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
	Pin4: RT/CT	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground. Operation to 500kHz is possible.
	Pin5: Ground	This pin is the combined control circuitry and power ground.
	Pin6: Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
	Pin7: Vcc	This pin is the positive supply of the control IC.
	Pin8: Vref	This is the reference output. It provides charging current for capacitor CT through resistor RT.

Thermal Data

Symbol	Description	Max.	Units
Rth j-amb	Thermal Resistance Junction-ambient	100	°C/W

Electrical Specifications

Parameter	Test Conditions	Min.	Typ.	Max.	Units
<i>Under-Voltage Lockout Section</i>					
Start Threshold		14.5	16	17.5	V
Min. Operating Voltage	After Turn On	8.5	10	11.5	V

Electrical Characteristics

Unless otherwise stated, specifications apply for $0 \leq T_a \leq 70^\circ\text{C}$ $V_{cc} = 15\text{V}$ (Note 1); $R_T = 680\Omega$, $C_T = 0.022\mu\text{F}$ for triangular mode, $R_T = 10\text{k}$, $C_T = 3.3\text{nf}$ for sawtooth mode

Parameter	Test Conditions	Min.	Typ.	Max.	Units
<i>Reference Section</i>					
Reference Output Voltage	$T_j = 25^\circ\text{C}, I_o = 1\text{mA}$	4.90	5	5.1	V
Line Regulation	$12\text{V} \leq V_{in} \leq 25\text{V}$	-	2.0	20	mV
Load Regulation	$1\text{mA} \leq I_o \leq 20\text{mA}$	-	3.0	25	mV
Temperature Stability	(Note 2)	-	0.2	-	mV/°C
Total Output Variation	Line, Load, Temp (Note 2)	4.82	-	5.18	V
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}, T_j = 25^\circ\text{C}$ (Note 2)	-	50	-	uV
Long Term Stability	$T_a = 125^\circ\text{C}, 1000\text{Hrs}$ (Note 2)	-	5	-	mV
Output Short current	$T_a = 25^\circ\text{C}$	-30	-100	-180	mA
<i>Oscillator Section</i>					
Frequency	$T_j = 25^\circ\text{C}$	47	52	57	KHz
	$T_{low} \leq T_a \leq T_{high}$	46	52	60	KHz
Frequency Chnge with Temperature	$12\text{V} \leq V_{cc} \leq 25\text{V}$	-	0.2	1	%
Frequency Change with Temperature	$T_{low} \leq T_a \leq T_{high}$ (Note 2)	-	5	-	%
	$T_j = 25^\circ\text{C}$	-	0.5	-	%
Oscillator Voltage Swing	Peak to Peak	-	1.7	-	V
Discharge Current	$T_j = 25^\circ\text{C}$	7.8	8.3	9.3	mA
	$T_{low} \leq T_a \leq T_{high}$	7.2	-	9.5	mA



Parameter	Test Conditions	Min.	Typ.	Max.	Units
<i>Oscillator Section</i>					
Frequency	Tj=25°C	47	52	57	KHz
	Tlow≤Ta≤Thigh	46	52	60	KHz
Frequency Chnge with Temperature	12V≤Vcc≤25V	-	0.2	1	%
Frequency Change with Temperature	Tlow≤Ta≤Thigh (Note 2)	-	5	-	%
	Tj=25°C	-	0.5	-	%
Oscillator Voltage Swing	Peak to Peak	-	1.7	-	V
Discharge Current	Tj=25°C	7.8	8.3	9.3	mA
	Tlow≤Ta≤Thigh	7.2	-	9.5	mA
<i>Error Amplifier Section</i>					
Voltage Feedback Input	Vo=2.5V	2.42	2.50	2.58	V
Input Bias Current	VFB=5.0V	-	-0.1	-2.0	uA
Open Loop Voltage Gain	2≤Vo≤4 V	65	90	-	dB
Unity Gain Bandwidth	Tj=25°C (Note 2)	0.7	1.0	-	MHz
Power Supply Rejection Ratio	12V≤Vcc≤25V	60	70	-	dB
Output Current	Sink (Vo=1.1V, VFB=2.7V)	2.0	12	-	mA
	Source (Vo=5.0V, VFB=2.3V)	-0.5	-1.0	-	mA
Output Voltage Swing High State	VFB=2.3V, RL=15K to ground	5	6	-	V
		Low State	VFB=2.7V, RL=15K to Vref	-	0.7
<i>Current Sense Section</i>					
Current Sense Input Voltage Gain	(Notes 3 & 4)	2.85	3.0	3.15	V/V
Maximum Current Sense Input Thresold	(Note 3)	0.9	1.0	1.1	V
Ppwer Supply Rejection Ratio	12V≤Vcc≤25V (Note 3)	-	70	-	dB
Input Bias Current		-	-2.0	-10	uA
Propagation Delay	Tj=25°C (Note 2)	-	150	300	nS
<i>Output Section</i>					
Output Voltage	Low State (Isink=20mA)	-	0.1	0.4	V
	Low State (Isink=200mA)	-	1.5	2.2	V
	High State (Isource=20mA)	13	13.5	-	V
	High State (Isource=200mA)	12	13.4	-	V
Output Voltage Rise Time	Tj=25°C, CL=1.0nF (Note 2)	-	50	150	nS
Output Voltage Fall Time	Tj=25°C, CL=1.0nF (Note 2)	-	50	150	nS
Output Voltage with UVLO Activated	Vcc=6V, Isink=1.0mA	-	-0.1	-1.1	V
<i>Total Device</i>					
Start-Up Current		-	0.1	0.5	mA
Operating Supply Current	Vpin2=Vpin3=0, RT=10K, CT=3.3nF	-	11	17	mA
Vcc Zener Voltage	Icc=25 mA	-	34	-	V

Note 1: Adjust Vcc above the start threshold before setting at 15V.

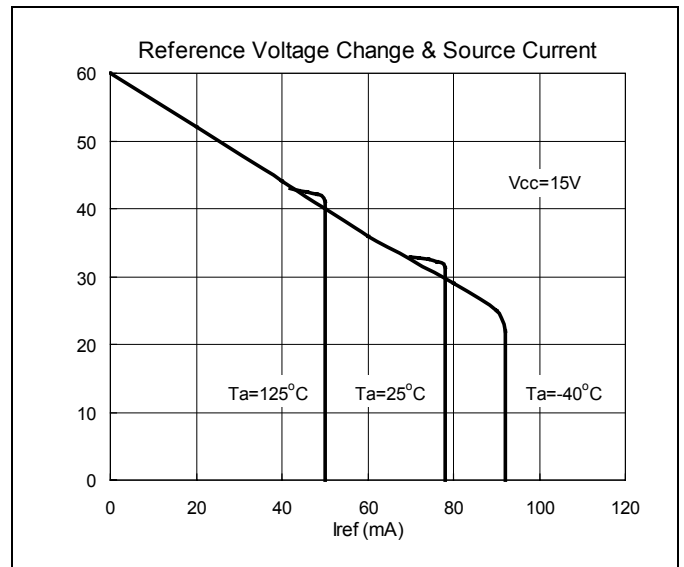
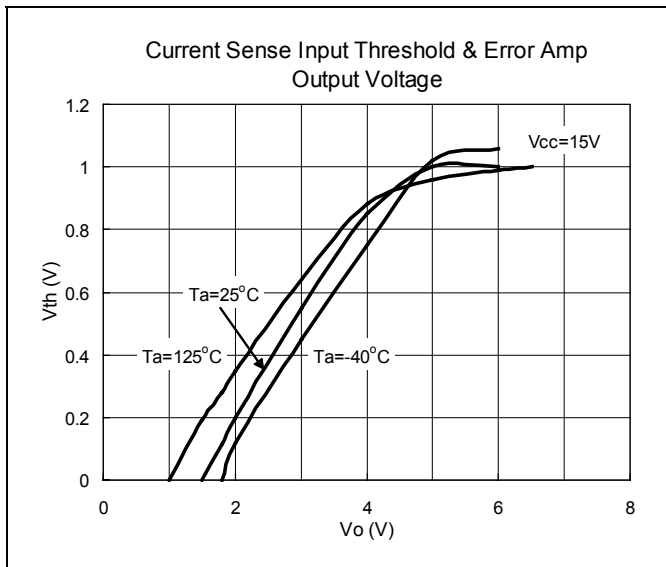
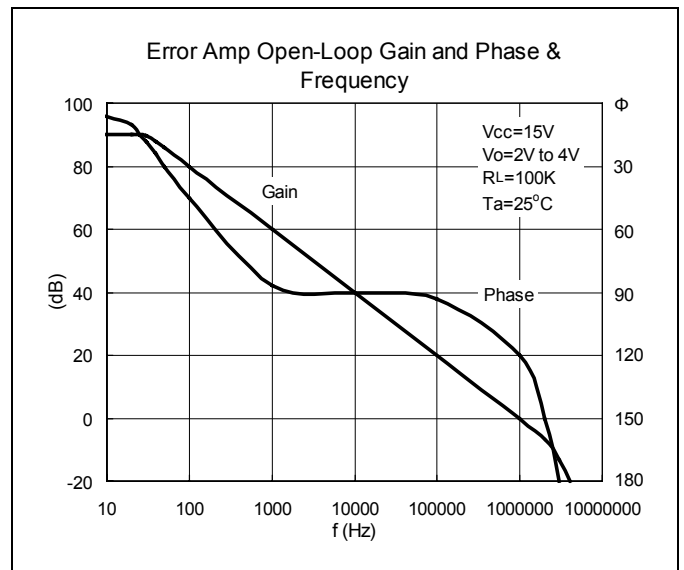
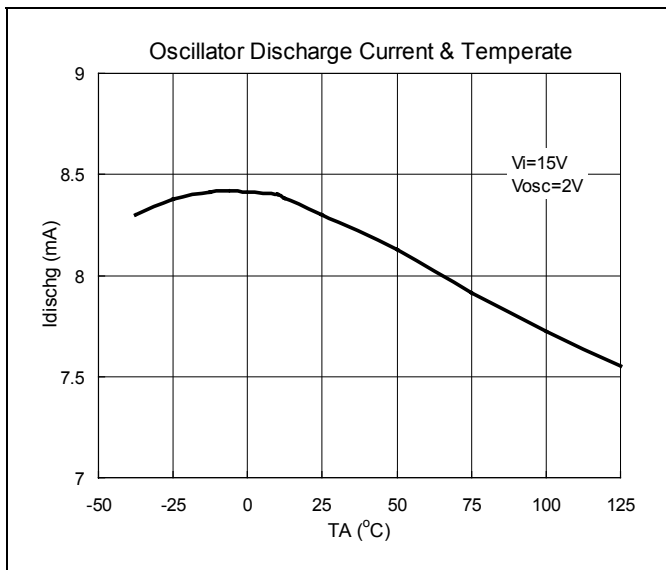
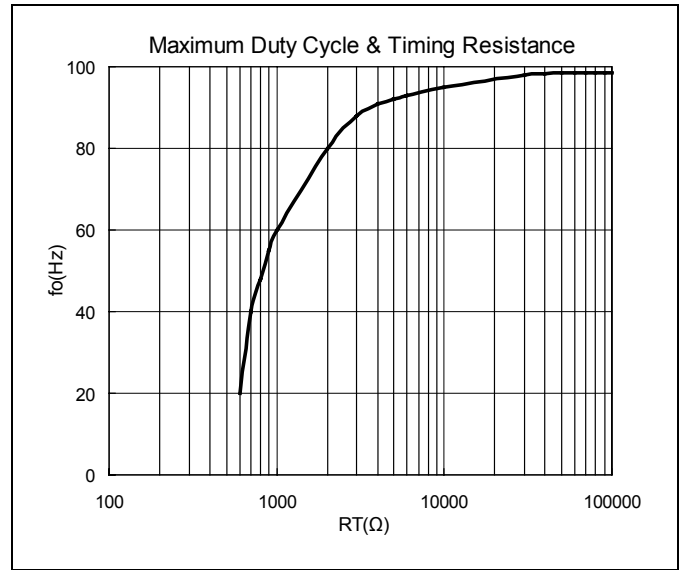
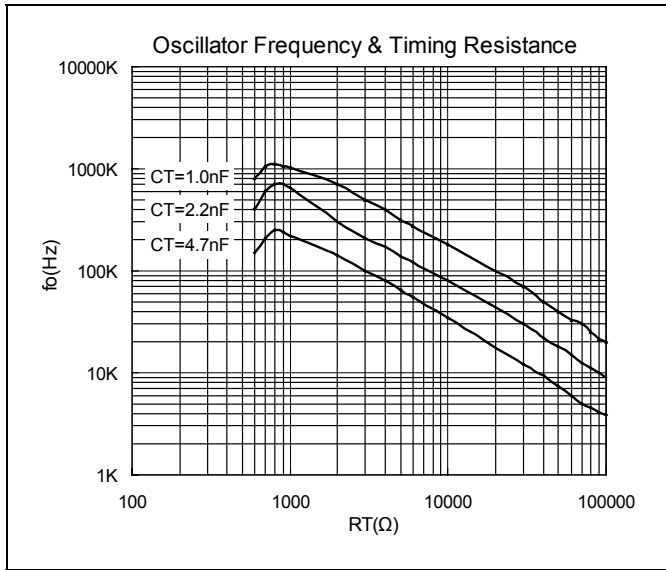
Note 2: These parameters, although guaranteed are not 100% tested in production.

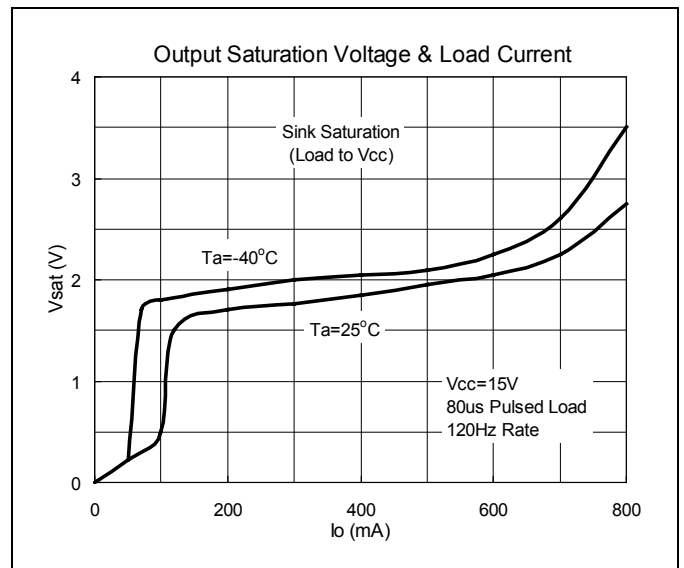
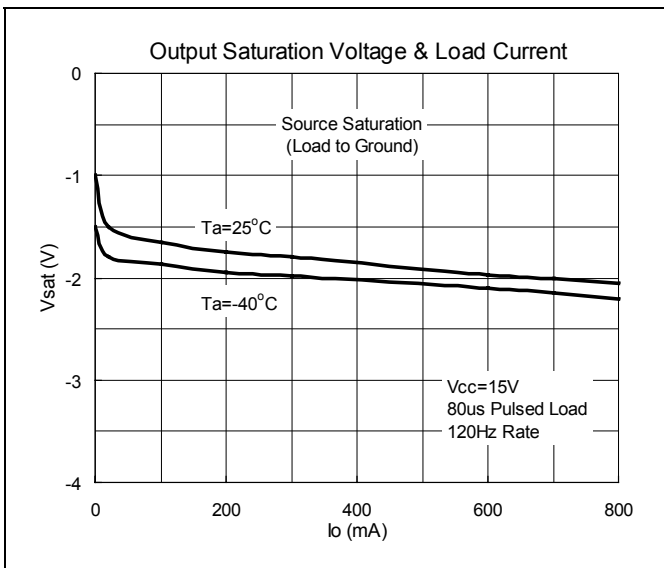
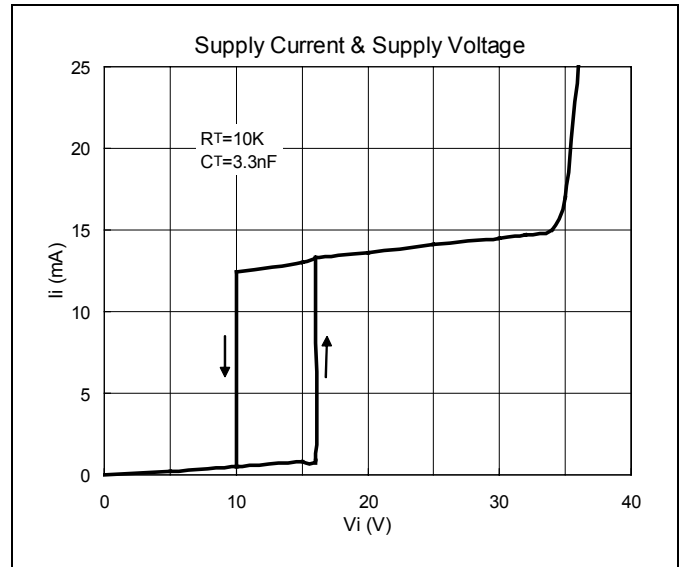
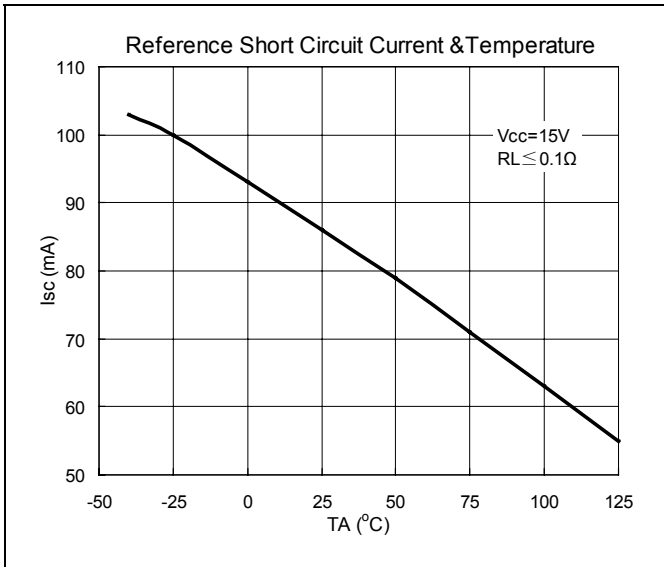
Note 3: Parameter measured at trip point of latch with Vpin2=0.

Note 4: Gain defined as: $A = V_{pin1}/V_{pin3}$, $0 \leq V_{pin3} \leq 0.8V$



Characteristics Curve

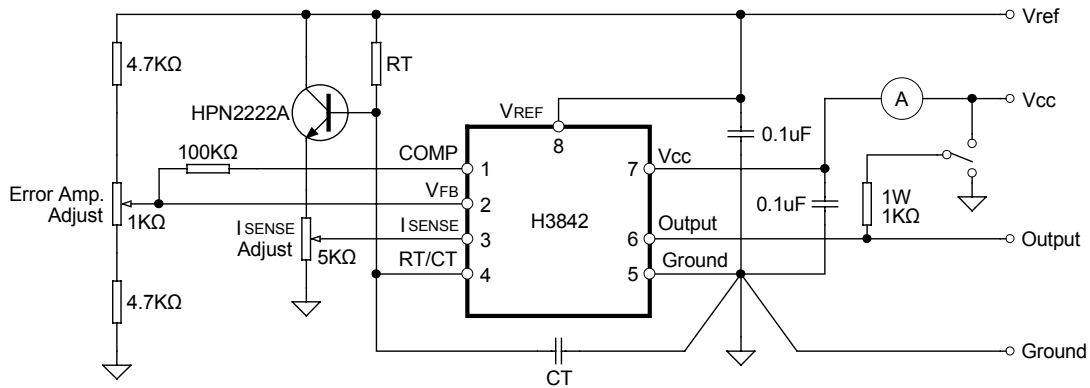






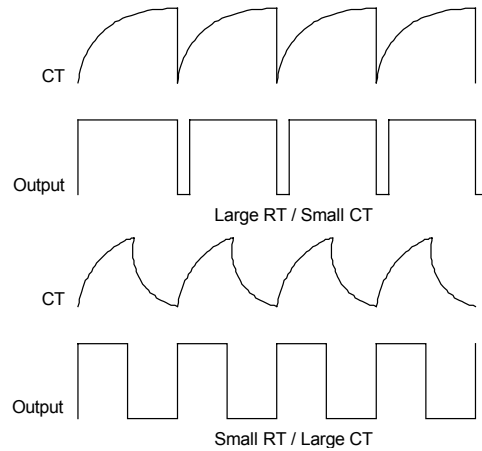
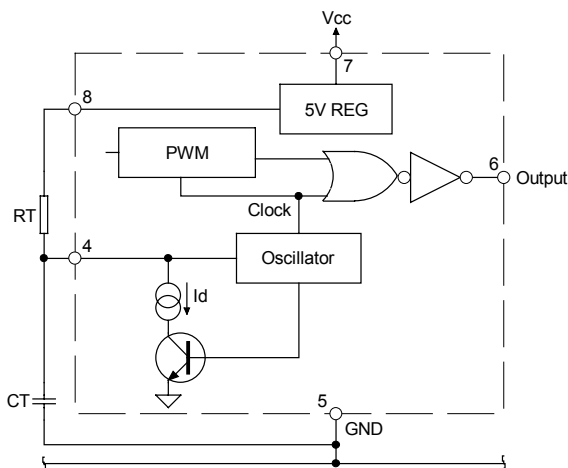
Application Information

Open Loop Test Circuit

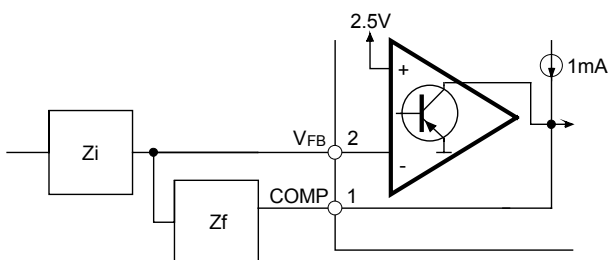


High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin5 in a single point ground. The transistor and 5KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin3.

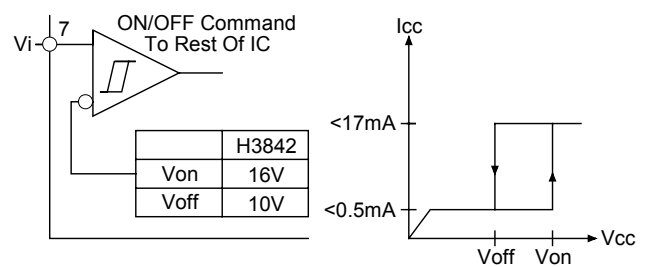
Oscillator and Output Waveforms



Error Amp Configuration

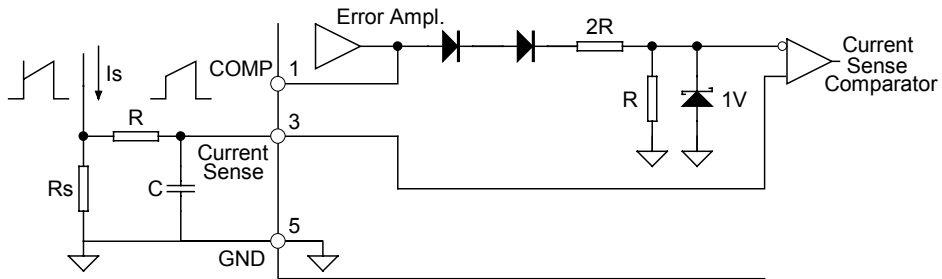


Under Voltage Lockout



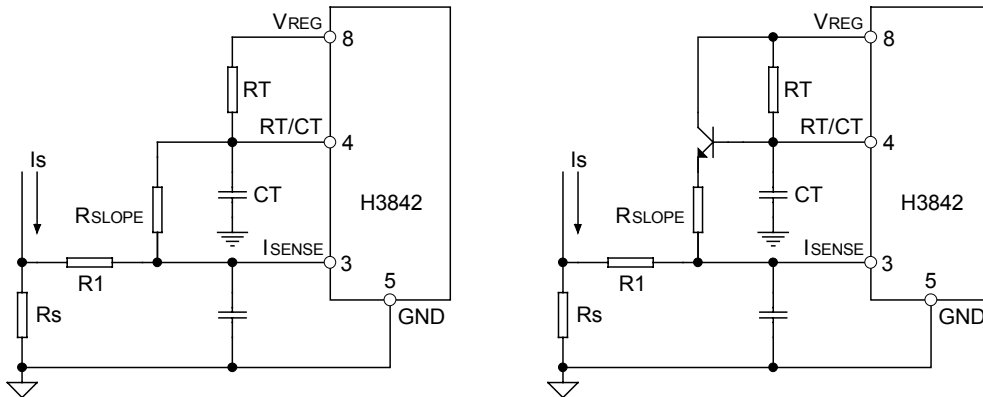


Current Sense Circuit

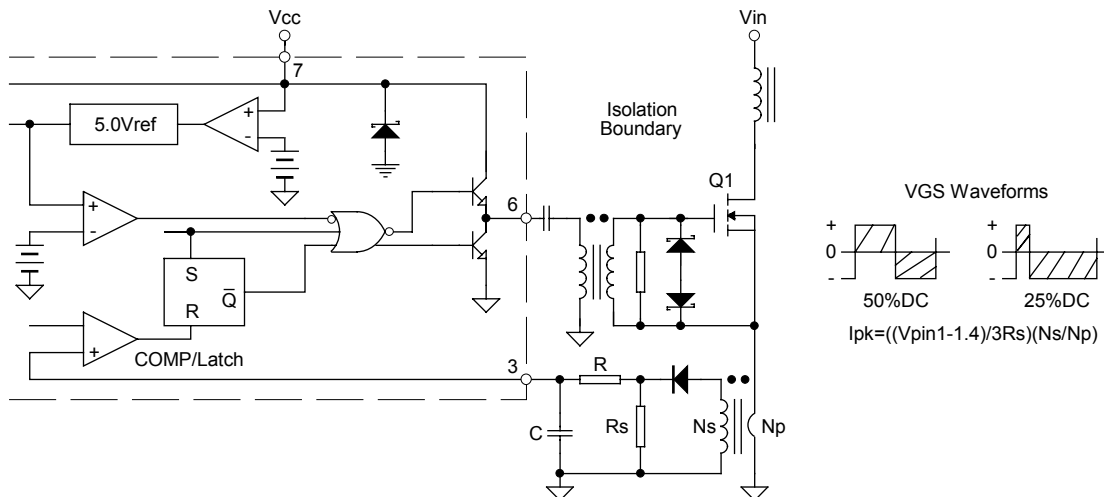


Peak current (I_s) is determined by the formula
 $I_s(\text{max.}) \approx 1V/R_s$
 A small RC filter may be required to suppress switch transients.

Slope Compensation Techniques

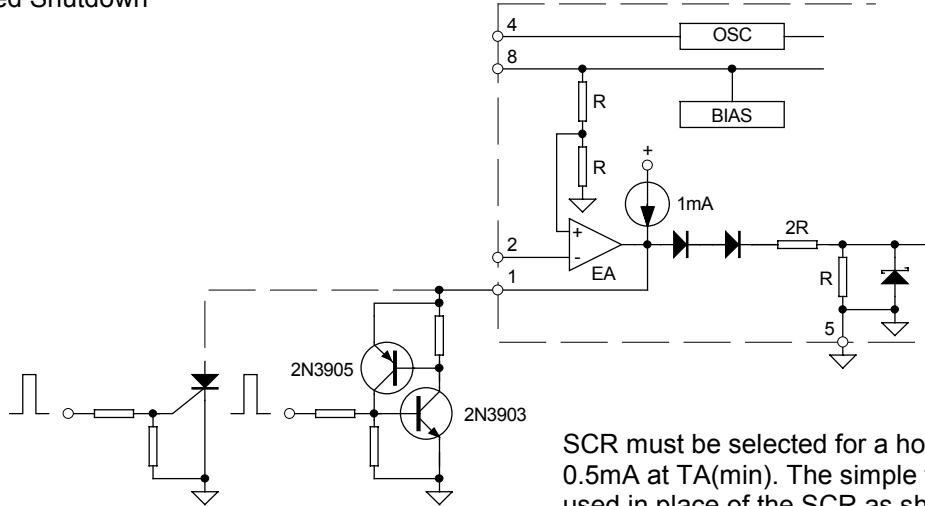


Isolated MOSFET Drive and Current Transformer Sensing



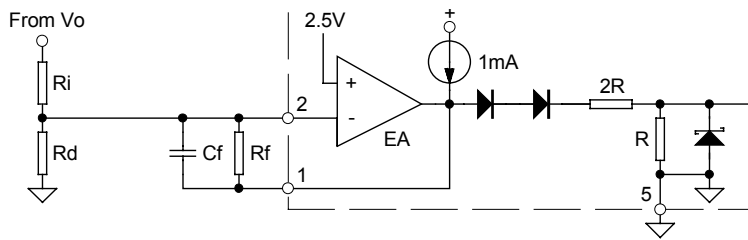


Latched Shutdown

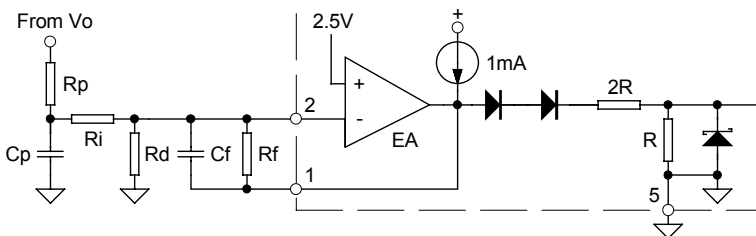


SCR must be selected for a holding current of less than 0.5mA at TA(min). The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10K.

Error Amplifier Compensation

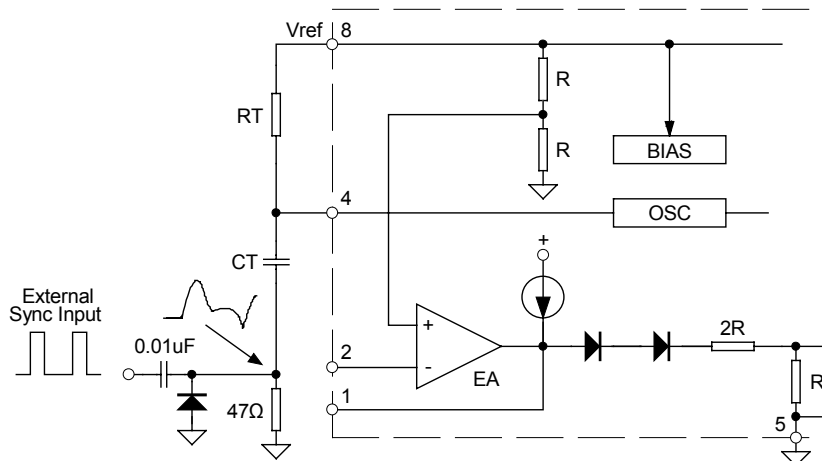


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

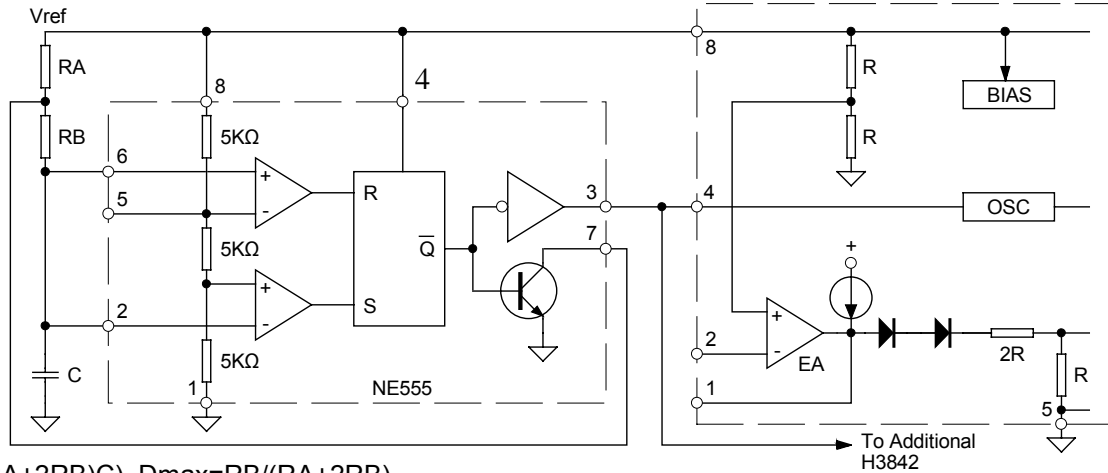
External Clock Synchronization



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300mV below ground

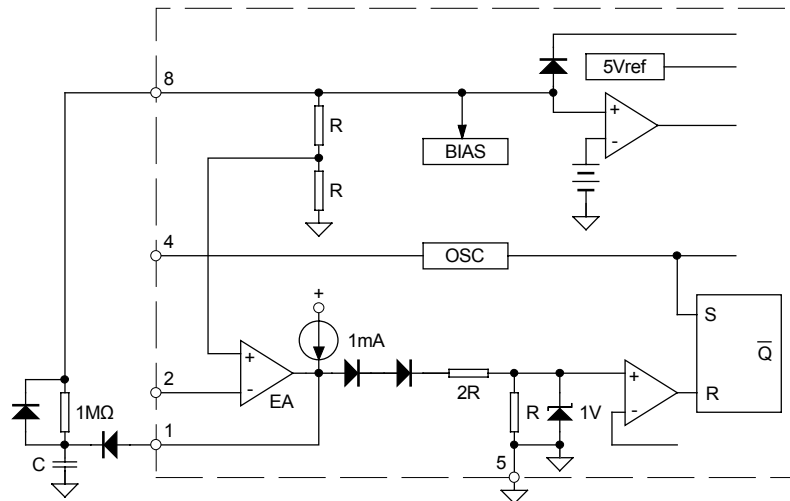


External Duty Cycle Clamp and Multi Unit Synchronization

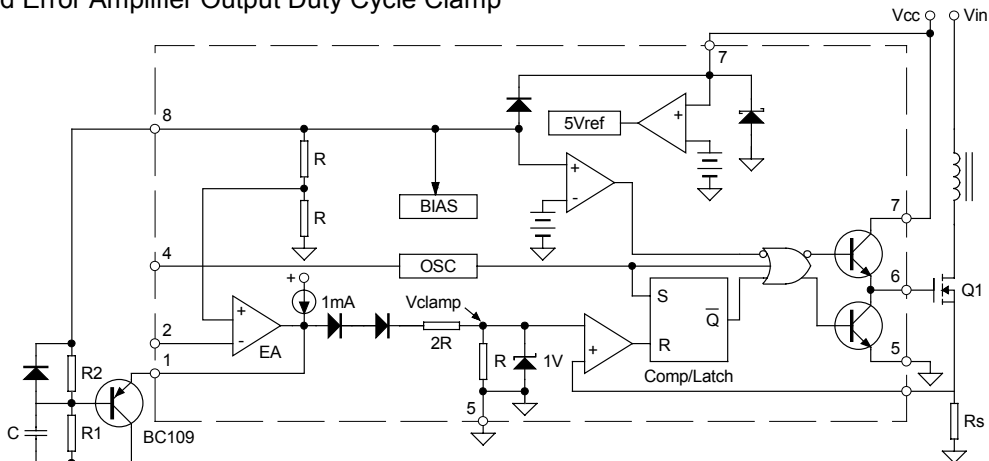


$$f = 1.44 / ((RA + 2RB)C), D_{max} = RB / (RA + 2RB)$$

Soft-Start Circuit



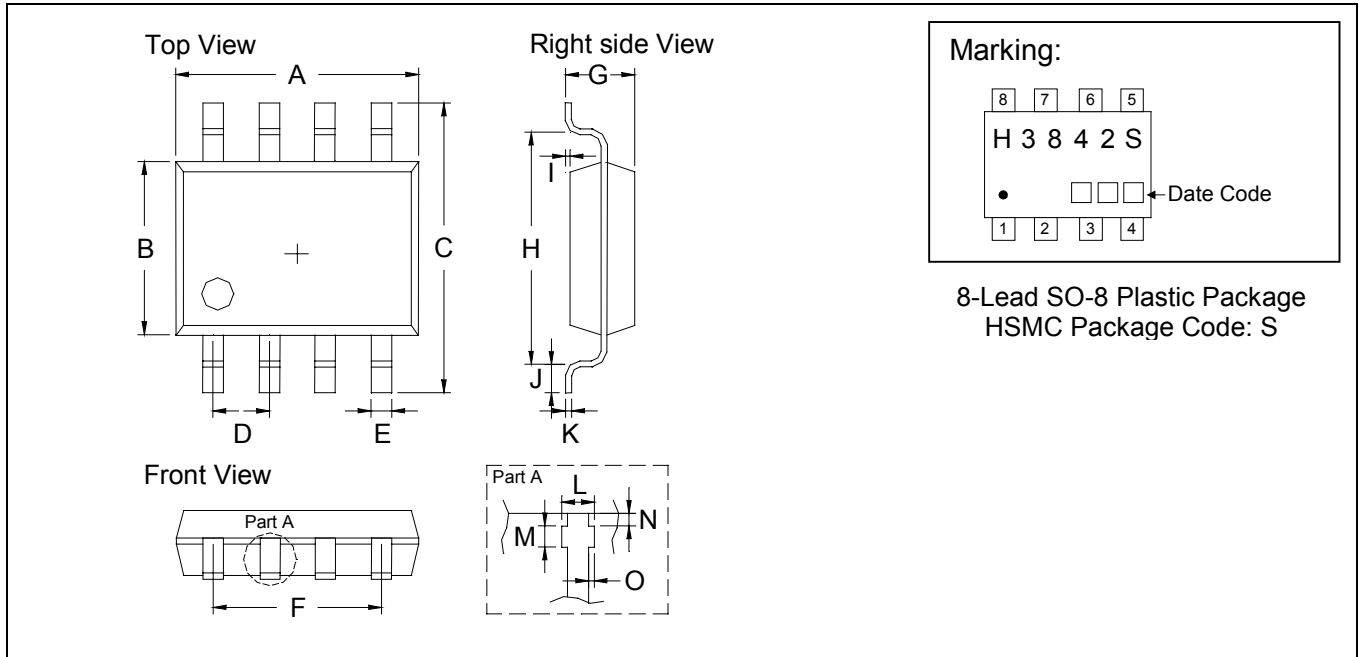
Soft-Start and Error Amplifier Output Duty Cycle Clamp



$$V_{clamp} = R1 / (R1 + R2) \text{ where } 0 < V_{clamp} < 1V, I_{pk(max)} = V_{clamp} / R_S$$



SO-8 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1.Dimension and tolerance based on our Spec. dated Aug. 01,1999.
 2.Controlling dimension: millimeters.
 3.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 4.If there is any question with packing specification or packing method, please contact your local HSMC sales office.

Material:

- Lead: 42 Alloy; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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